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INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____ - _____

070-2757-00

First Printing APR 1979

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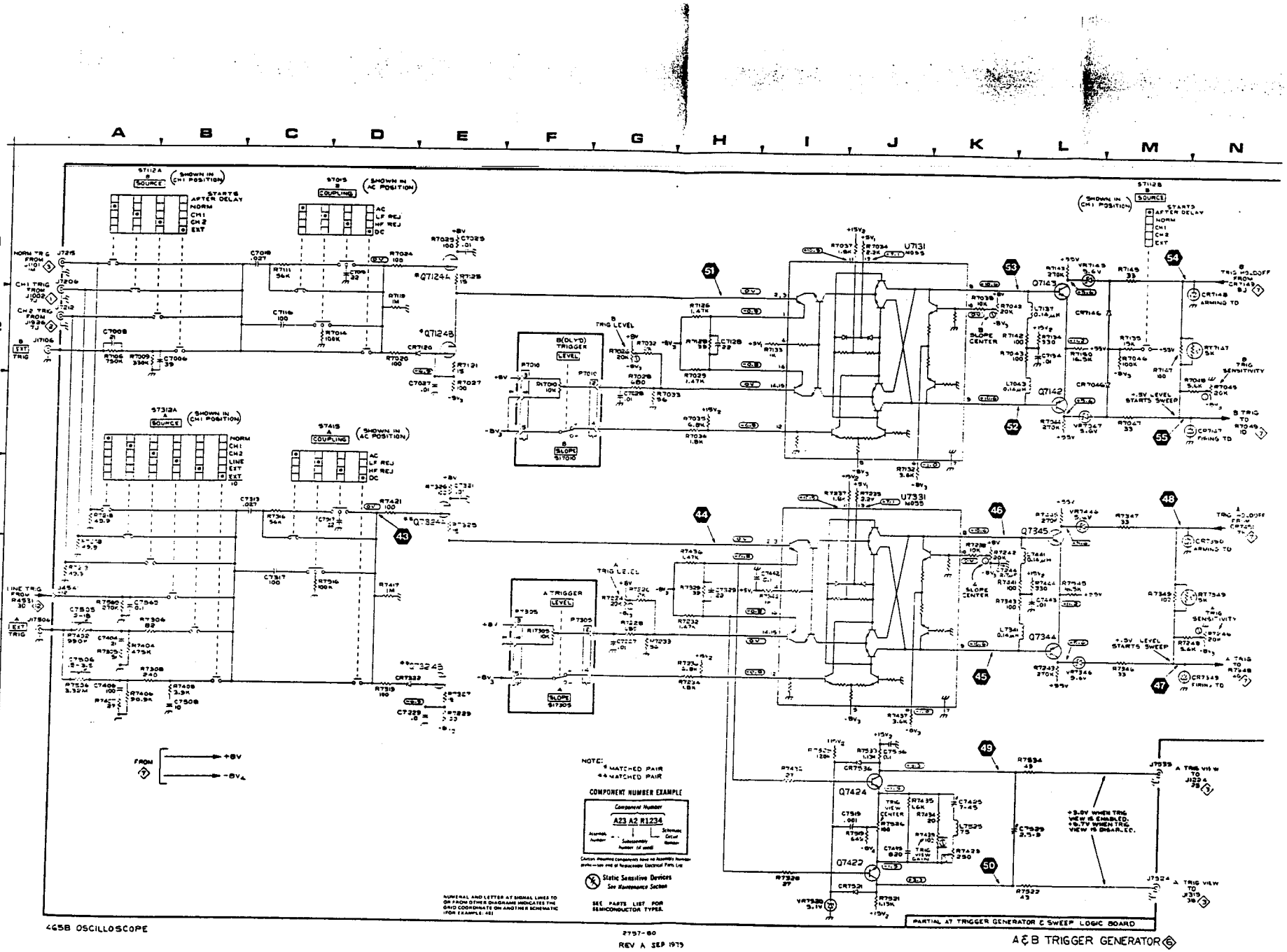


4658 OSCILLOSCOPE

2757-80
REV A SEP 1979

A & B TRIGGER GENERATOR

A & B TRIGGER GENERATORS

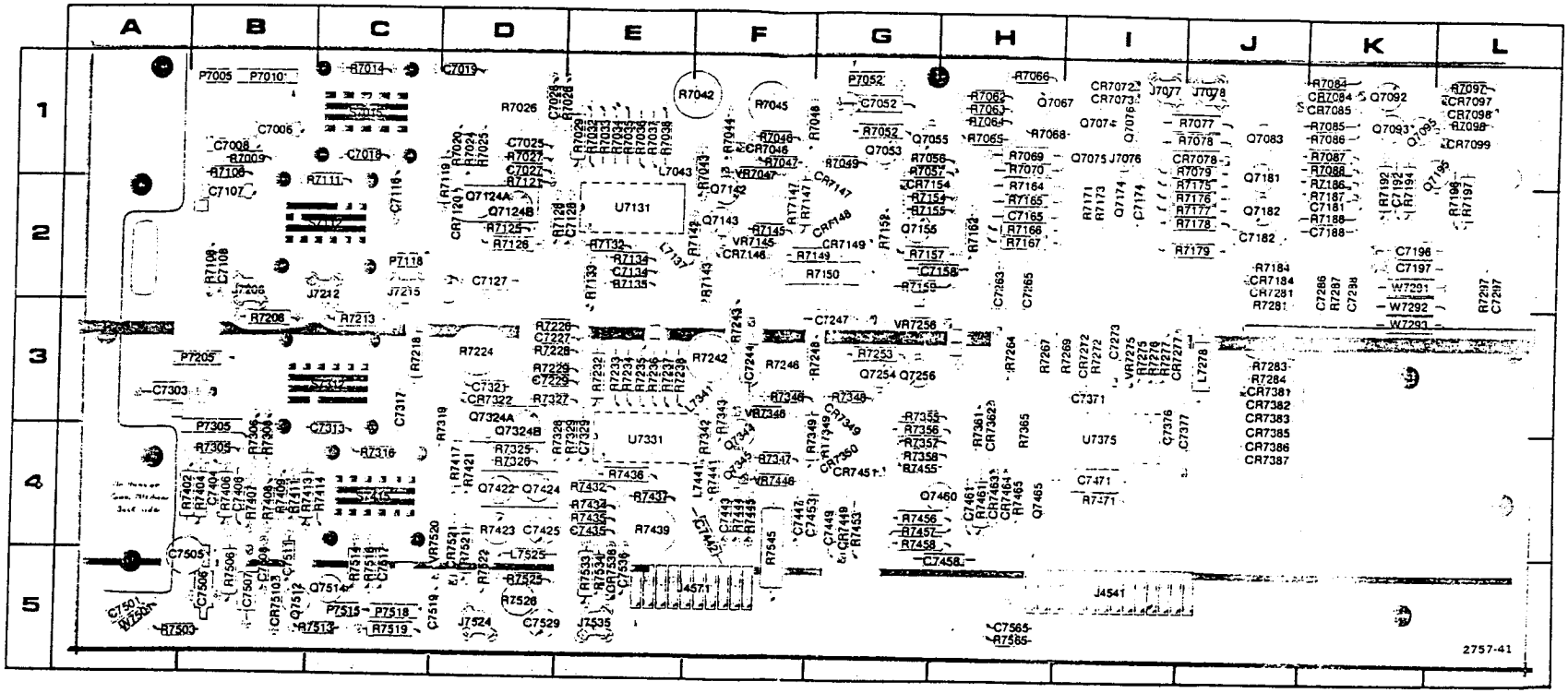
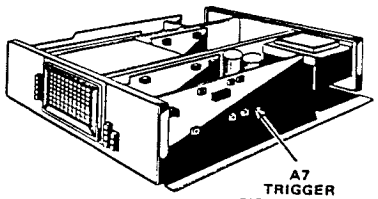
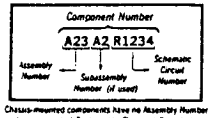


Figure 8-6. A7 Trigger Generator and Sweep Logic circuit board.

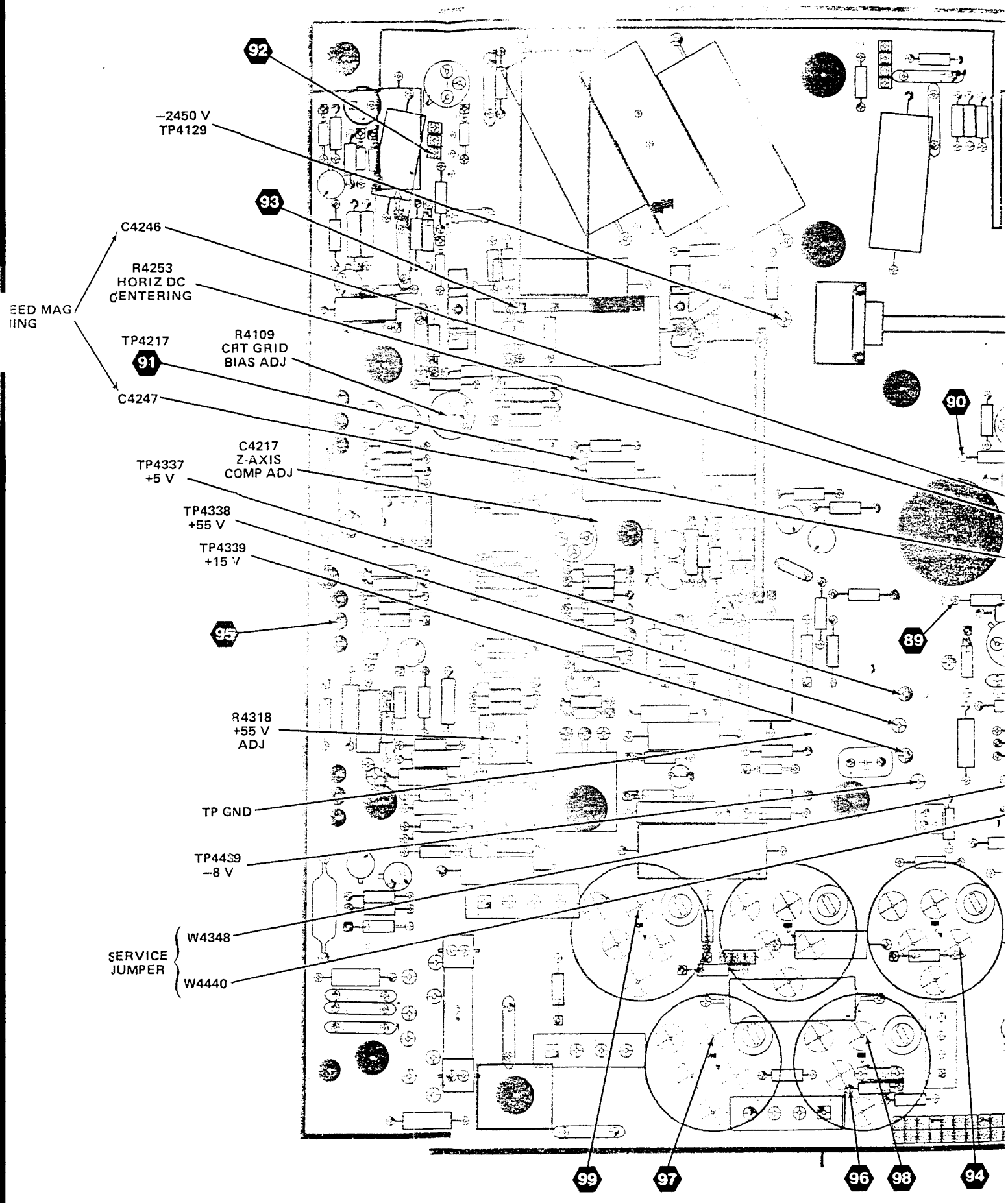


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

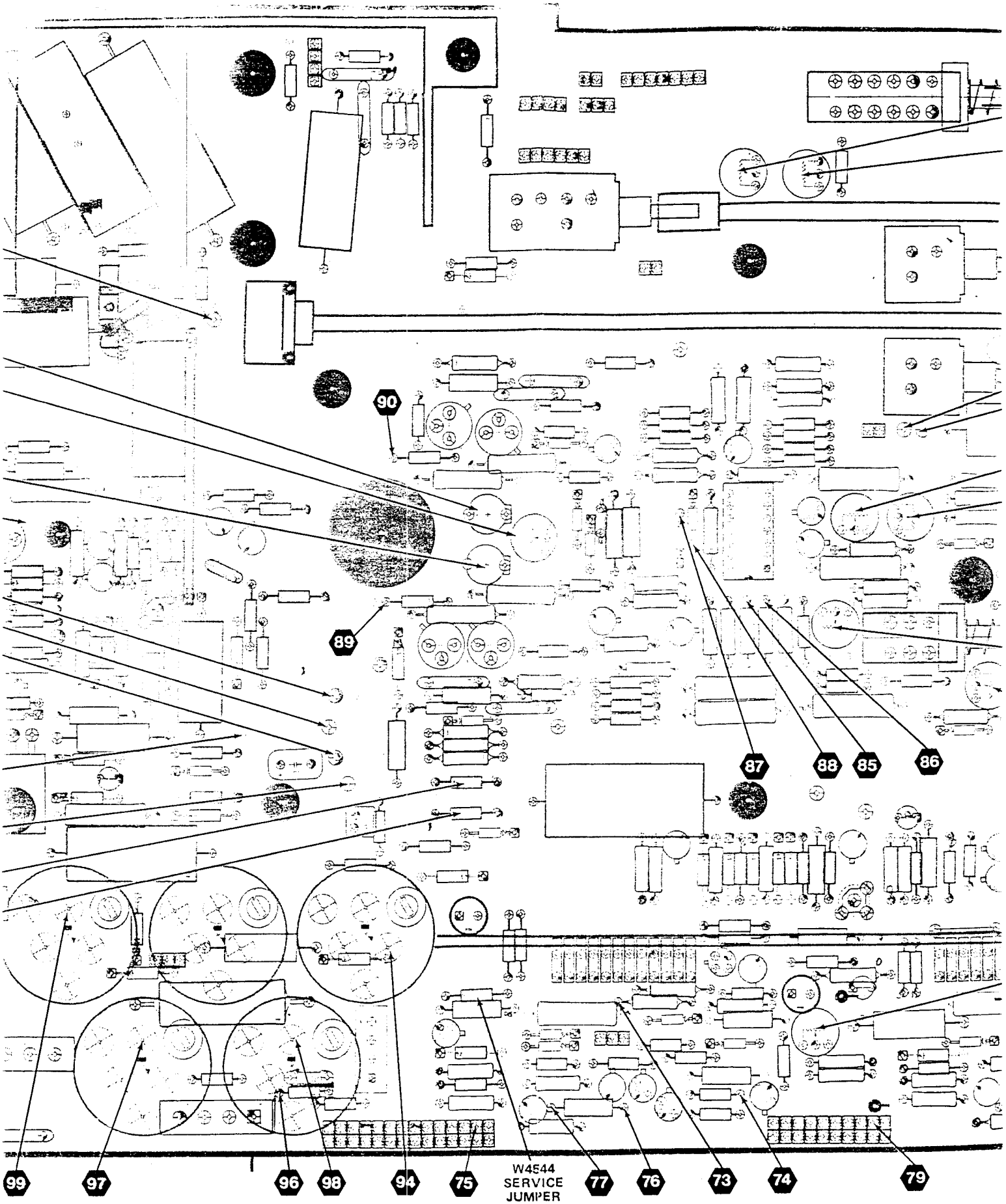


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



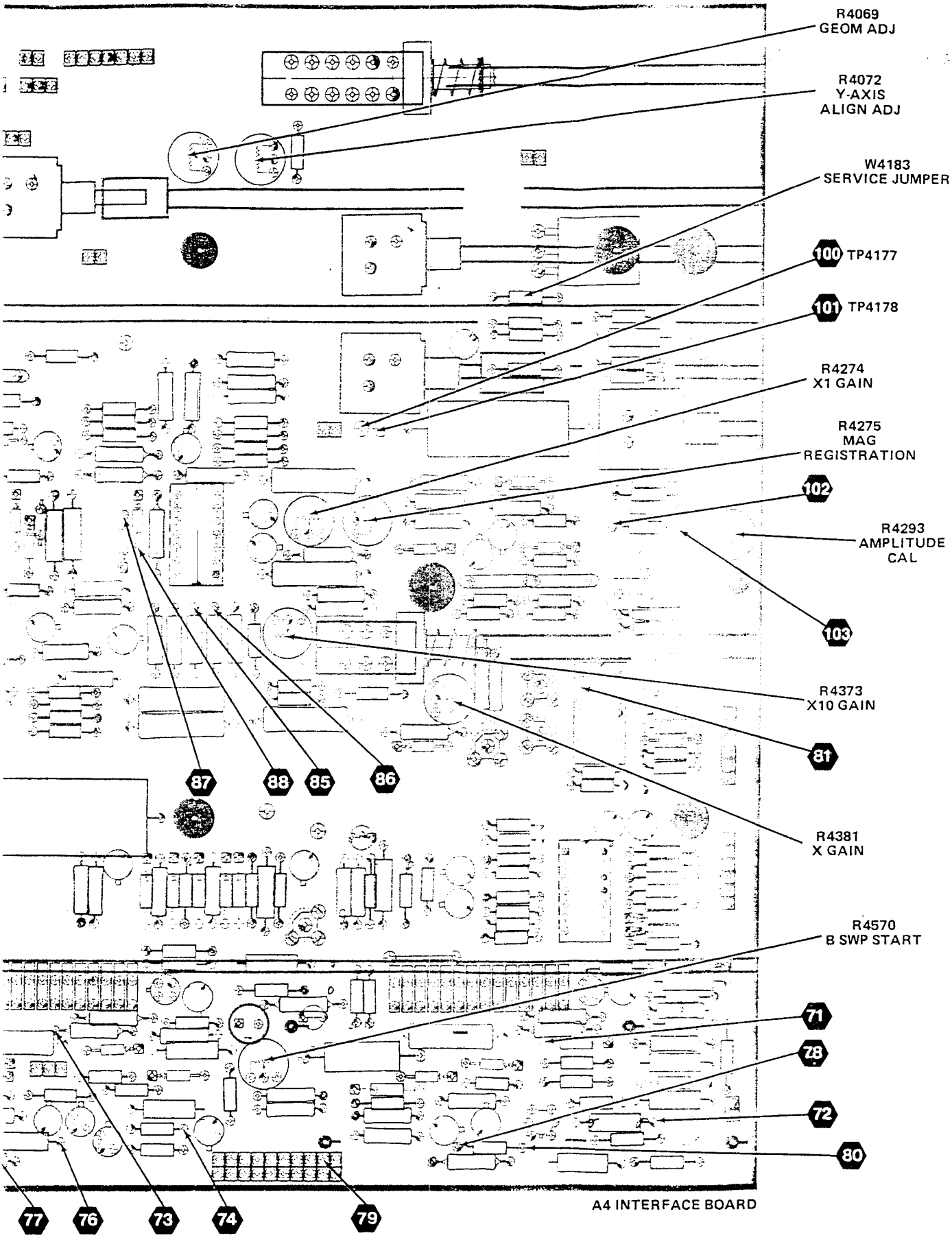
REV A SEP 1979

Figure 8-



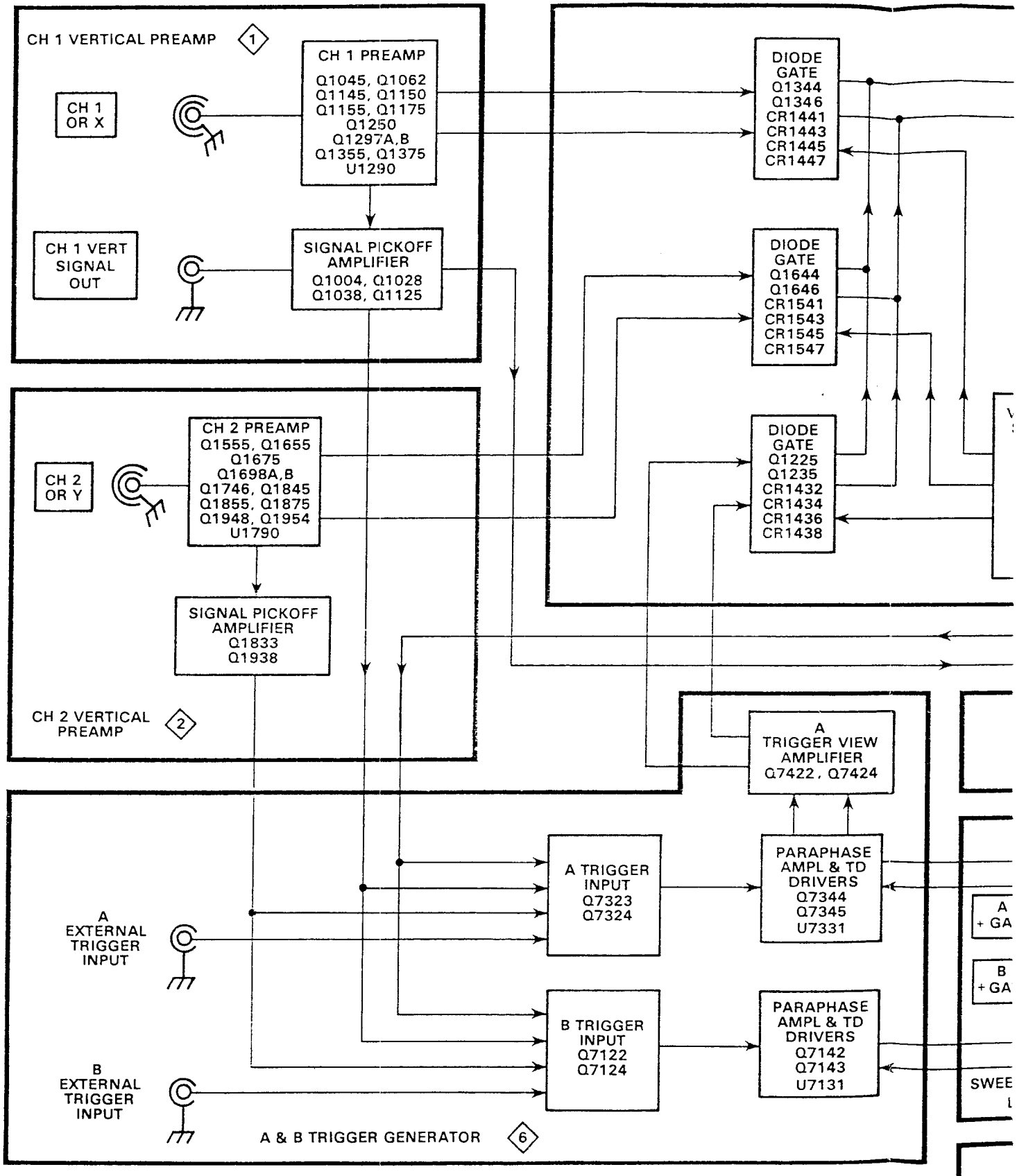
REV A SEP 1979

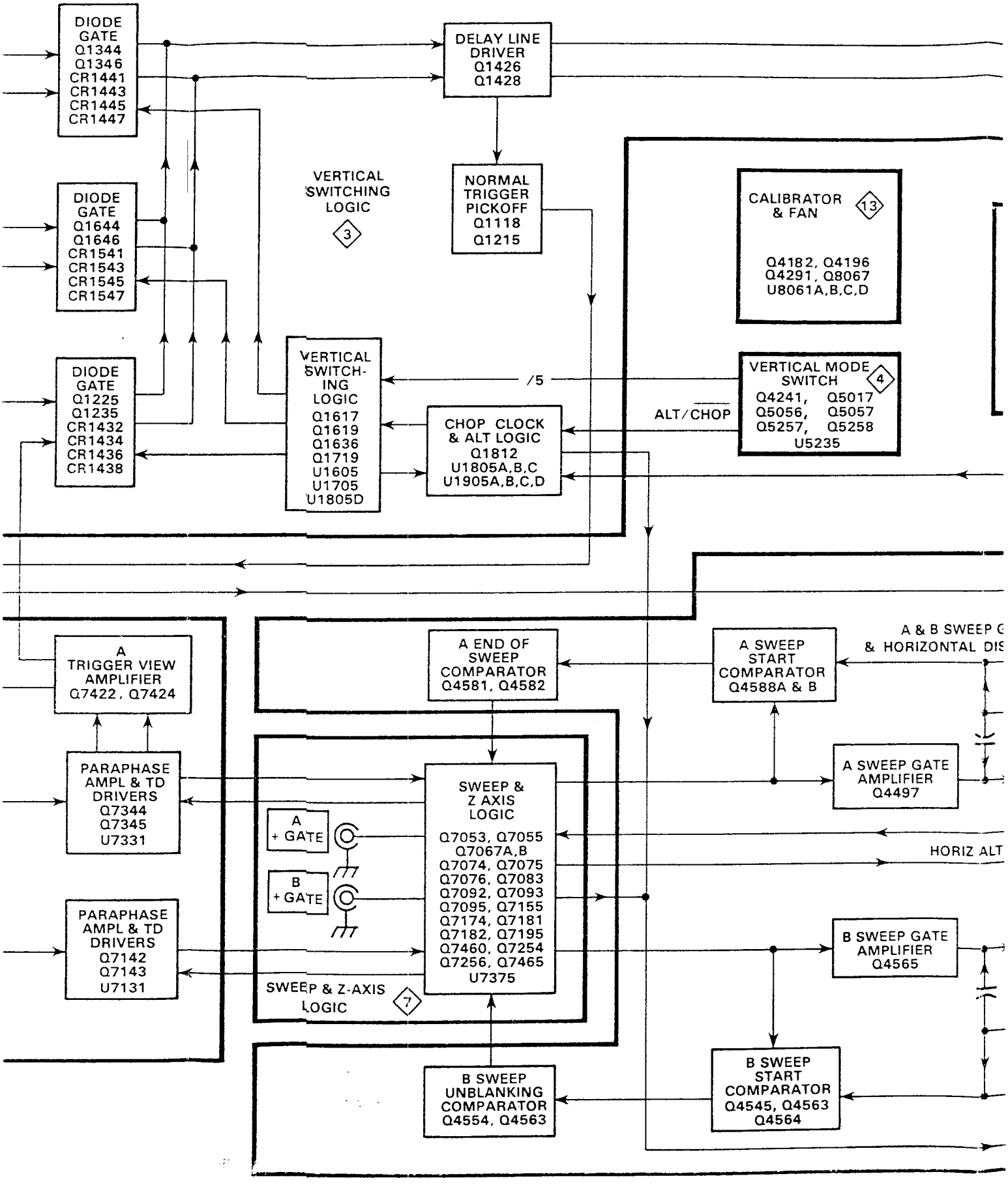
Figure 8-10. Interface circuit board adjustment locations.

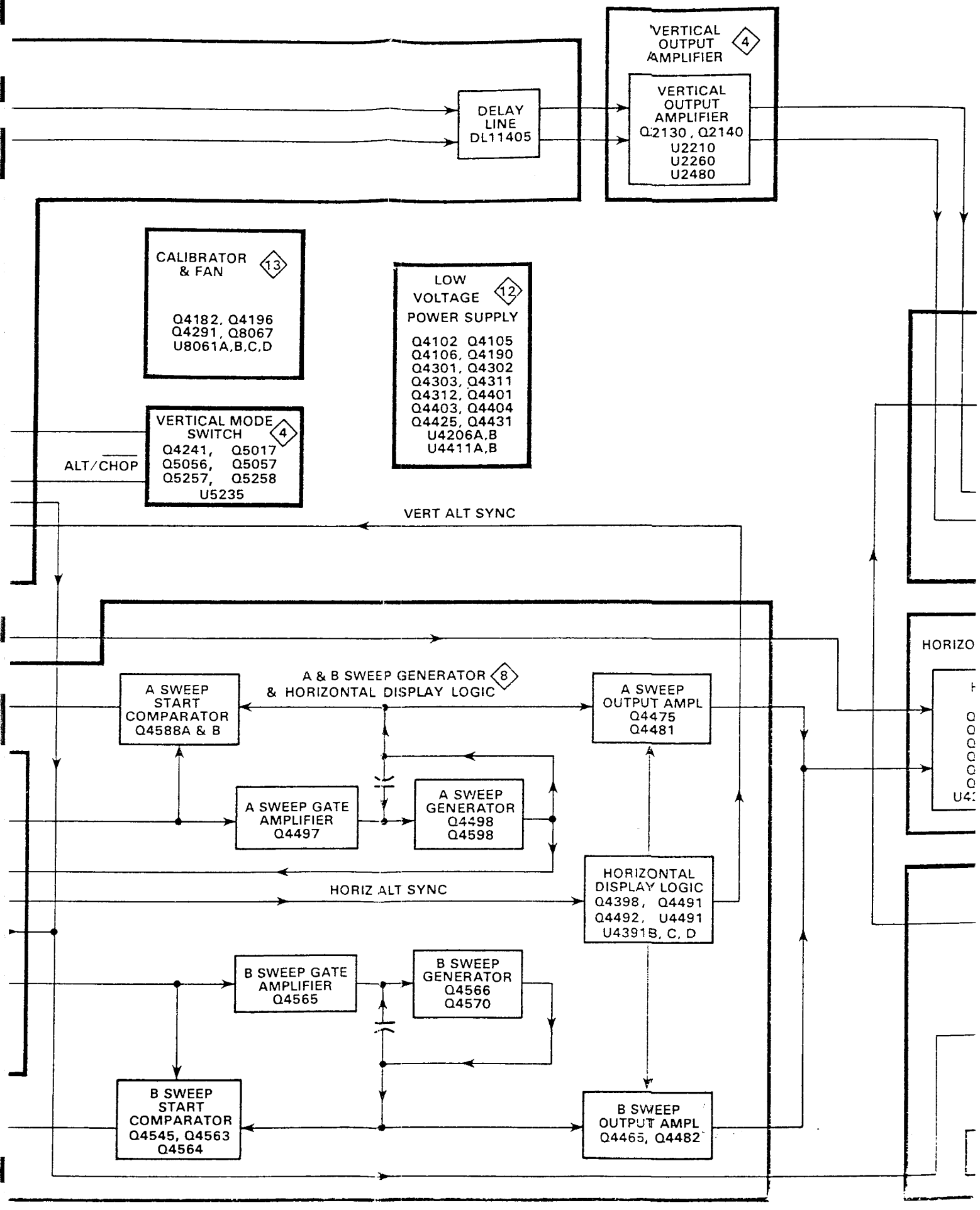


2757-111

oard adjustment locations.


CH 1 VERTICAL PREAMP
1
CH 1 OR X
CH 1 PREAMP
Q1045, Q1062
Q1145, Q1150
Q1155, Q1175
Q1250
Q1297A,B
Q1355, Q1375
U1290
CH 1 VERT SIGNAL OUT
SIGNAL PICKOFF AMPLIFIER
Q1004, Q1028
Q1038, Q1125
DIODE GATE
Q1344
Q1346
CR1441
CR1443
CR1445
CR1447
DIODE GATE
Q1644
Q1646
CR1541
CR1543
CR1545
CR1547
CH 2 OR Y
CH 2 PREAMP
Q1555, Q1655
Q1675
Q1698A,B
Q1746, Q1845
Q1855, Q1875
Q1948, Q1954
U1790
SIGNAL PICKOFF AMPLIFIER
Q1833
Q1938
DIODE GATE
Q1225
Q1235
CR1432
CR1434
CR1436
CR1438
CH 2 VERTICAL PREAMP
2
A TRIGGER VIEW AMPLIFIER
Q7422, Q7424
A TRIGGER INPUT
Q7323
Q7324
PARAPHASE AMPL & TD DRIVERS
Q7344
Q7345
U7331
A EXTERNAL TRIGGER INPUT
B TRIGGER INPUT
Q7122
Q7124
PARAPHASE AMPL & TD DRIVERS
Q7142
Q7143
U7131
B EXTERNAL TRIGGER INPUT
A & B TRIGGER GENERATOR
6


DIODE GATE Q1344 Q1346 CR1441 CR1443 CR1445 CR1447
DELAY LINE DRIVER Q1426 Q1428
VERTICAL SWITCHING LOGIC
3
NORMAL TRIGGER PICKOFF Q1118 Q1215
DIODE GATE Q1644 Q1646 CR1541 CR1543 CR1545 CR1547
CALIBRATOR & FAN
13
Q4182, Q4196 Q4291, Q8067 U8061A,B,C,D
VERTICAL SWITCH-ING LOGIC Q1617 Q1619 Q1636 Q1719 U1605 U1705 U1805D
/5
VERTICAL MODE SWITCH
4
Q4241, Q5017 Q5056, Q5057 Q5257, Q5258 U5235
DIODE GATE Q1225 Q1235 CR1432 CR1434 CR1436 CR1438
CHOP CLOCK & ALT LOGIC Q1812 U1805A,B,C U1905A,B,C,D
ALT/CHOP
A TRIGGER VIEW AMPLIFIER Q7422, Q7424
A END OF SWEEP COMPARATOR Q4581, Q4582
A SWEEP START COMPARATOR Q4588A & B
A & B SWEEP G
& HORIZONTAL DIS
PARAPHASE AMPL & TD DRIVERS Q7344 Q7345 U7331
SWEEP & Z AXIS LOGIC Q7053, Q7055 Q7067A,B Q7074, Q7075 Q7076, Q7083 Q7092, Q7093 Q7095, Q7155 Q7174, Q7181 Q7182, Q7195 Q7460, Q7254 Q7256, Q7465 U7375
A SWEEP GATE AMPLIFIER Q4497
A + GATE
B + GATE
HORIZ ALT
PARAPHASE AMPL & TD DRIVERS Q7142 Q7143 U7131
B SWEEP GATE AMPLIFIER Q4565
SWEEP & Z-AXIS LOGIC
7
B SWEEP UNBLANKING COMPARATOR Q4554, Q4563
B SWEEP START COMPARATOR Q4545, Q4563 Q4564


VERTICAL OUTPUT AMPLIFIER 4
DELAY LINE DL11405
VERTICAL OUTPUT AMPLIFIER Q2130, Q2140 U2210 U2260 U2480
CALIBRATOR & FAN 13
Q4182, Q4196 Q4291, Q8067 U8061A,B,C,D
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ALT/CHOP
VERT ALT SYNC
A & B SWEEP GENERATOR & HORIZONTAL DISPLAY LOGIC 8
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A SWEEP OUTPUT AMPL Q4475 Q4481
A SWEEP GATE AMPLIFIER Q4497
A SWEEP GENERATOR Q4498 Q4598
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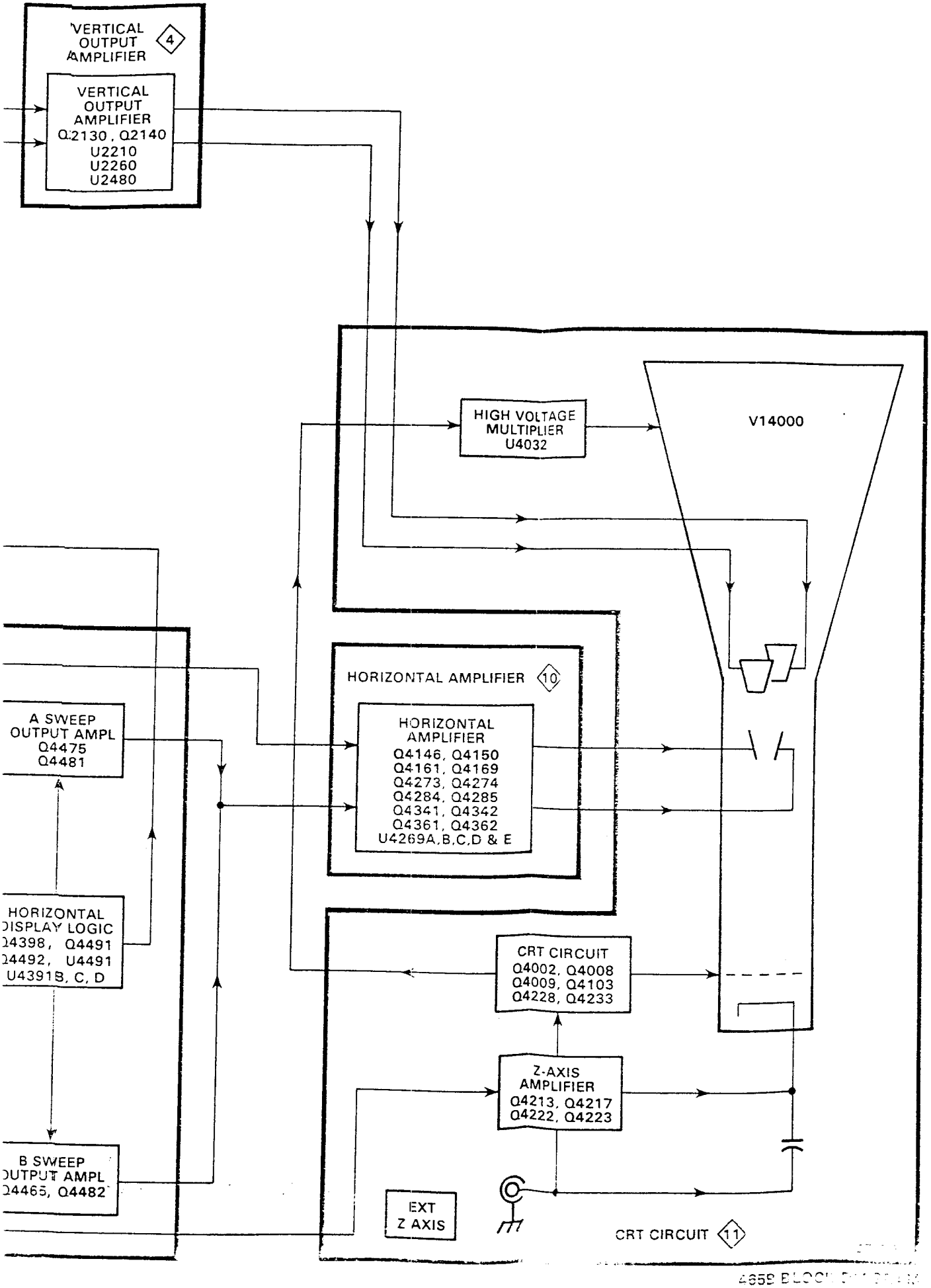
HORIZ ALT SYNC
B SWEEP GATE AMPLIFIER Q4565
B SWEEP GENERATOR Q4566 Q4570
B SWEEP START COMPARATOR Q4545, Q4563 Q4564
B SWEEP OUTPUT AMPL Q4465, Q4482
HORIZO


VERTICAL OUTPUT AMPLIFIER
4
VERTICAL OUTPUT AMPLIFIER
Q2130, Q2140
U2210
U2260
U2480
HIGH VOLTAGE MULTIPLIER
U4032
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HORIZONTAL AMPLIFIER
10
HORIZONTAL AMPLIFIER
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Q4341, Q4342
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Q4481
HORIZONTAL DISPLAY LOGIC
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Q4492, U4491
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Q4465, Q4482
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EXT Z AXIS
CRT CIRCUIT
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465B
OSCILLOSCOPE

WITH OPTIONS
(B060000 AND UP)

SERVICE

INSTRUCTION MANUAL

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WITH OPTIONS
(B060000 AND UP)
SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-4273-00
Product Group 40

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First Printing MAR 1982
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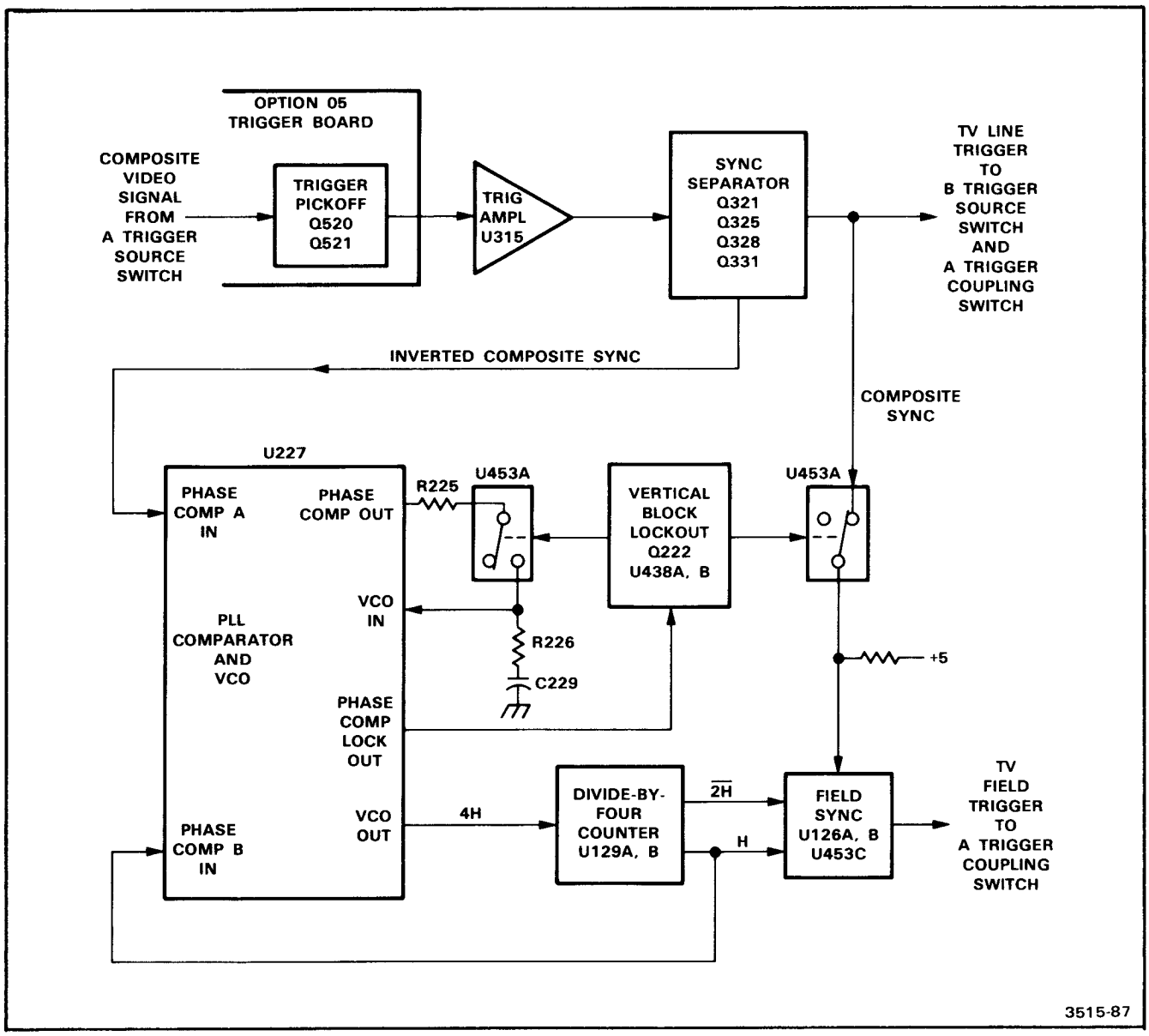

Figure 7-4. 465B Option 05, simplified block diagram.

P7575 and P2810 to the Trigger Amplifier. Diode CR7510 prevents high-amplitude, negative-going signals from damaging the input of Q7512. High-amplitude, positive-going signals are limited by the gate-to-drain current that flows when the source-gate junction of Q7512 becomes forward biased.

Trigger Amplifier

Trigger Amplifier U315 and associated components provide adequate drive for the Sync-Separator. Output from the Trigger Amplifier stage is fed to Q325, the Sync Separator circuitry input transistor. Feedback resistor R310 (from U315, pin 8 to U315, pin 3) controls the gain of U315 for low-amplitude signals, while R311, CR310, and CR311 control the gain for higher-amplitude signals.

Sync Separator

The Sync Separator circuit (composed of Q321, Q325, Q328, Q331, and associated components) is arranged as a wide-band, high-gain, self-biasing clipping amplifier that performs several functions.

1. Positive video information is removed (stripped) from incoming sync-negative, composite video signals.

2. Negative sync tips are clipped to eliminate possible noise or, in some systems, subsidiary signals.

3. The "middle" portion of the resulting composite sync is amplified for use as the A and B Sweep (TV LINE) sync. The amplified signal is further processed by the Field Selection circuitry to obtain the TV Field trigger signal to the A Sweep trigger circuitry.

Sync Stripper. With no signal applied (quiescent state), Q325 and Q321 are biased to produce approximately +5 V on the Q321 collector, and Q331 is biased into saturation. The collector of Q331 will be at approximately 0 V.

When the composite video signal from U315 is applied to the base of Q325 (via R324 and C323) the negative-sync portion increases the forward bias of Q325, thereby lowering the Q325 emitter voltage. This negative-going emitter voltage, applied directly to the base of Q321, reduces the forward bias on Q321 and allows the Q321 collector voltage level to rise. Thus, the negative-sync portion of the composite video signal is amplified and invertd. However, transistor Q321 remains saturated during the positive voltage changes of the Q321 collector, so the negative sync tips are not passed on to the composite sync bus.

The amount of dc feedback applied to the base of Q325 is determined by the sync-tip amplitude. Current through CR333 rapidly charges C329, and the forward bias on Q328 increases. The increased current flow through Q328 applies a negative dc feedback to Q325 through the parallel combination of R327, C321, and R321, thereby limiting the positive output level of Q321.

The negative transition of the sync pulse output from Q321 is applied to C329 through R331 and R332, producing a relatively long time-constant-discharge path. Between sync pulses, the charge on C329 reduces only a small amount, and the dc feedback remains at the level determined by the sync tip amplitude. If the signal amplitude were to reduce, the sync tip amplitude would also be less. The negative feedback generated would be reduced, increasing the gain and adjusting to a lower input signal level.

The gain for positive-going portions of the input signal is over 100 (limited primarily by the finite gain of Q321). The positive video portions of the input signal saturate Q321 whenever the peak-to-peak input amplitude exceeds approximately 60 mV. Any signal applied to Q321 while it is saturated will not be amplified. This results in the positive portion of the composite-video signal being clipped. However, the negative-sync portion of the input signal is amplified to nearly 6 V peak-to-peak and inverted at the output of Q321. This inverted composite sync signal is fed via R409 and R408 to the Phase Comparator A input of U227 to control the phase-locked-loop oscillator, and applied via R326 to the base of Sync Clipper Q331.

Sync Clipper. Transistor Q331 passes a signal only during a narrow input signal level range. During the quiescent state, and also whenever the sync tips drive the collector of Q321 positive, Q331 is saturated. On the negative transition of a sync pulse, Q331 comes out of saturation as the Q321 output signal level drops through +4 V, but it becomes cutoff as the signal level continues to drop through +3 V. Sync Clipper Q331 then amplifies only the middle portion of the sync signal, clipping off the sync tips and any excursions of color subcarrier peaks that may have extended into the sync area. The amplified composite sync is fed to a voltage divider composed of R101 and R102 to reduce the signal amplitude to the correct level for application via P2834 to the A and B Trigger Generator circuits. This composite-sync signal is also applied via U453A, a MOSFET bilateral switch, to the Field Selection circuitry.

Field Selection

The Field Selection circuitry consists of the following.

1. A phase-locked-loop oscillator, operating at four times the television horizontal line rate (4H).

2. A sync-block-lookout circuit that opens the error-correction input to the phase-locked-loop oscillator during the vertical sync interval to prevent equalizing pulses, serrations, or (in some systems) the absence of horizontal sync pulses from affecting the oscillator frequency.

3. Sampling circuits that, after each horizontal sync pulse, interrogate the state of the composite sync bus at the one-quarter and three-quarter points in a line interval and then generate the FIELD output sync signal.

Phase-Locked Loop. The phase-locked loop is composed of U227, a CMOS phase comparator and voltage-controlled oscillator (VCO), and U129A and B, a divide-by-four counter. The VCO oprates at four times the horizontal frequency, while the output of U129A and B is one-fourth the VCO frequency (the horizontal frequency). The minimum VCO frequency is set by C228 to less than 40 kHz, or four times the line rate of a 405-line, 50-Hz video system. Range-setting resistor R224 extends the upper frequency range to above 144 kHz (four times the line rate of a 1201-line, 60-Hz system).

Inverted composite sync is applied to U227 at pin 14, the Phase Comparator A input. The VCO output is divided by

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465B
OSCILLOSCOPE AND DM44 DIGITAL MULTIMETER OPERATORS

INSTRUCTION MANUAL

Tektronix, Inc.
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Beaverton, Oregon 97077

070-2756-00

Serial Number _____ First Printing, MAR 1979

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b. to repair damage resulting from improper use or from connecting the product to incompatible equipment;
c. if personnel other than Tektronix representatives modify the hardware or software.

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MAGNIFIED SWEEP DISPLAY

1. Preset instrument controls and obtain a Normal Sweep Display.

2. Adjust the horizontal POSITION control to move the area to be magnified to within the center graticule division of the crt (0.5 division on each side of the center vertical graticule line). Change the TIME/DIV switch setting as desired.

3. Push the X10 MAG switch (on) and adjust the horizontal POSITION control for precise positioning of the magnified display. Divide the TIME/DIV setting by 10 to determine the magnified sweep rate.

DELAYED SWEEP DISPLAY

1. Preset instrument controls and obtain a Normal Display.

NOTE

Differential time measurements and measurements using the TIME or 1/TIME functions of the DM44 are invalid when the B Trigger SOURCE switch is not set to STARTS AFTER DELAY.

2. Set the HORIZ DISPLAY switch to A INTEN and the B Trigger SOURCE switch to STARTS AFTER DELAY.

3. Pull out on the B TIME/DIV knob and turn clockwise from counterclockwise stop until the intensified zone is the desired length. Adjust the INTENSITY and B INTENSITY controls as needed to make the intensified zone distinguishable from the rest of the display. If your instrument is equipped with a DM44, select a function other than TIME or 1/TIME for a single delayed sweep. Dual delayed displays are discussed in step 7.

4. Adjust the DELAY TIME POSITION control to move the intensified zone to cover the portion of the display that will be displayed in delayed form.

5. Set the HORIZ DISPLAY switch to B DLY'D. The intensified zone adjusted in steps 3 and 4 is now displayed in delayed form. The delayed sweep rate is indicated by the dot on the B TIME/DIV knob.

6. To obtain a delayed display with less jitter, set the B Trigger SOURCE switch to the same position as the A Trigger SOURCE switch and adjust the B LEVEL control for a stable display.

7. If your instrument is equipped with a DM44, delayed displays of two vertical channel signals can be obtained at the same time. The DM44 will indicate the time difference between the delayed displays. To obtain two delayed displays, select the TIME function and set the VERT MODE to ALT, CH 1 and CH 2. The DELAY TIME POSITION control is used to position both delayed displays. The Δ TIME control positions only the Channel 2 delayed display.

ALTERNATE SWEEP DISPLAY

1. Preset instrument controls and obtain a Normal Sweep Display.

2. Pull out on the B TIME/DIV knob to unlock it and turn clockwise to the desired sweep rate. If the instrument is equipped with a DM44, select a function other than TIME or 1/TIME.

3. Set the HORIZ DISPLAY switch to ALT. Set B (DLY'D) TRIGGER SOURCE to STARTS AFTER DELAY. Adjust Channel 1 POSITION and TRACE SEP as required to display A Sweep above B Sweep. This will provide a display that alternates between A INTEN trace (upper) and B DLY'D trace (lower). Adjust B INTENSITY as necessary to view the B DLY'D trace (lower).

the baseline to the bottom graticule line. If a negative voltage is to be measured, position the baseline to the top graticule line.

4. Switch the AC-GND-DC switch to DC. Measure the divisions of vertical deflection between the reference line and the desired point on the waveform (see Figure 15).

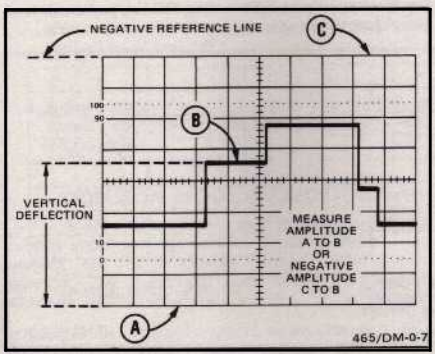

Figure 15. Instantaneous voltage measurement.

5. Calculate instantaneous voltage, using the following formula:

Instantaneous Voltage	=	vertical distance (divisions)	X	polarity (+ or −)	X	VOLTS/DIV switch setting

Also include the attenuation factor of the probe being used, if it is not a 10X scale-factor-switching probe.

EXAMPLE: The vertical distance measured is 4.6 divisions (see Figure 15). The waveform is above the reference line, and the VOLTS/DIV switch is set to 2.

Substituting the given values:

Instantaneous Voltage = 4.6 X (+1) X 2 V = +9.2 volts.

ALGEBRAIC ADDITION

With the VERT MODE switch in the ADD position, the waveform displayed is the algebraic sum of the signals applied to the Channel 1 and Channel 2 inputs (CH 1 + CH 2). If the Channel 2 INVERT switch is depressed, the waveform displayed is the difference of the signals applied to the Channel 1 and Channel 2 inputs (CH 1 − CH 2). The

OPTION 07
EXTERNAL DC OPERATION

SPECIFICATION

Electrical characteristics and performance requirements listed in the Specification section of this manual are applicable to the 465B Option 07 oscilloscope with the following exceptions or additions:

DC REQUIREMENTS. Either 11.5 to 14 volts or 22 to 28 volts. Operation with 11.5 to 14 volts excludes graticule light function and Option 05. Operating range may be extended to 15 volts or 30 volts with a series dropping resistor. Maximum elevation for + or – power lead is 50 volts with respect to oscilloscope chassis or ground.

CONTROLS AND CONNECTORS

Mode Switch — Three-position switch located adjacent to the Line Voltage Selector switch on the right side panel and used to select the proper input power to the 465B.

AC — Permits application of ac power to the oscilloscope power switch.

DC 12 — Permits operation of the instrument from an external 12-volt source.

DC 24 — Permits operation of the instrument from either an external 24-volt power source or from the 1106 Battery Pack, which may be mechanically attached to the oscilloscope.

DC Input Connector — Used for connecting external dc power source to the 465B Option 07; located on rear panel.

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DM44 DIGITAL MULTIMETER

WITH OPTIONS

SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-2036-01
Product Group 40

Serial Number _____

First Printing SEP 1976
Revised AUG 1982

INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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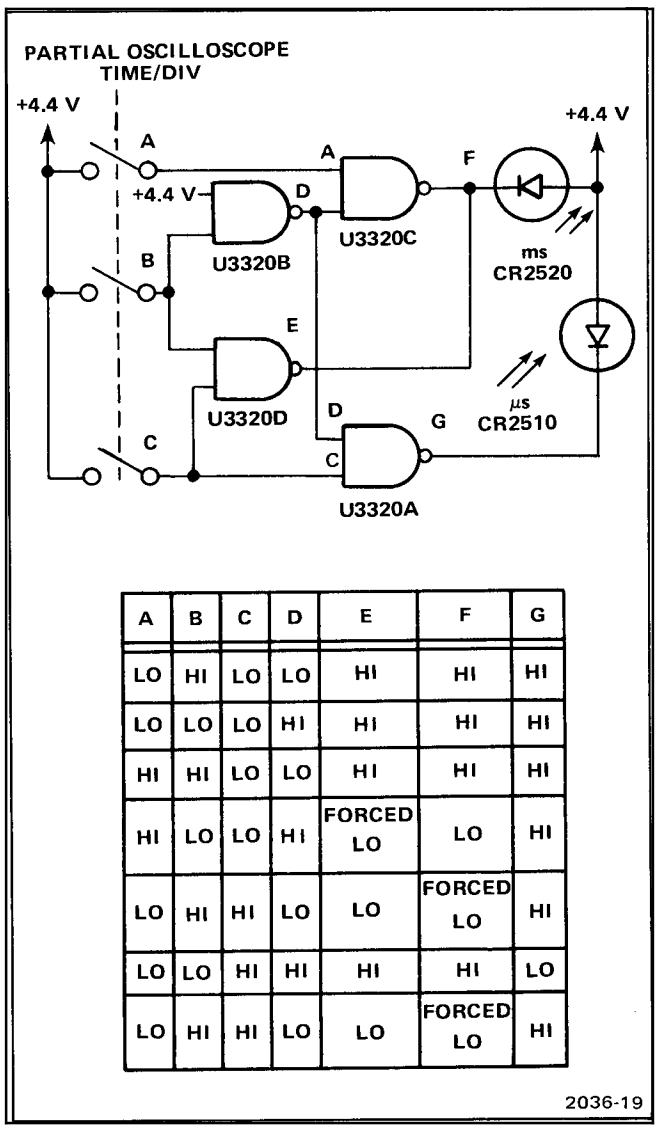
MS AND μS LOGIC 5

The ms and μs indicators are controlled by U3323 in the TIME function and by U3320 in the 1/TIME function. To do this, the supply voltage to U3320 is disconnected in the TIME function and the supply voltage to U3323 is disconnected in the 1/TIME function.

Figure 4-19 shows a simplified diagram and truth table of the ms and μs Logic in the 1/TIME function. Notice that the last condition is invalid. The oscilloscope TIME/DIV settings which produce this condition are not usable. The supply voltage to U3323 is disconnected in the 1/TIME function. Therefore, U3323 can be ignored.



A	B	C	D	E	F	G
LO	HI	LO	LO	HI	HI	HI
LO	LO	LO	HI	HI	HI	HI
HI	HI	LO	LO	HI	HI	HI
HI	LO	LO	HI	FORCED LO	LO	HI
LO	HI	HI	LO	LO	FORCED LO	HI
LO	LO	HI	HI	HI	HI	LO
LO	HI	HI	LO	LO	FORCED LO	HI

Fig. 4-19. Simplified diagram of ms and μs Logic when in the 1/TIME function.

Figure 4-20 shows a simplified diagram of the ms and μs Logic in the TIME function. The supply voltage to U3320 is disconnected in the TIME function. Therefore, U3320 can be ignored.

TIME AND 1/TIME AUTORANGE LOGIC 5

The Autorange Logic operates only in the TIME and 1/TIME functions. Figure 4-21 shows a simplified diagram of the TIME and 1/TIME Autorange Logic.

U3301C and U3301D are connected as an RS flip-flop. Normally the R and S inputs are both HI. With a HI on both inputs, the output state is not disturbed. A LO is needed on one of the inputs to set or reset the flip-flop.

Underrange Condition

The maximum net count from U3340 never allows bit four of digit four to go HI. When an underrange condition occurs, circuitry within U3340 causes pin 13 of U3340 (bit four) to go HI at the same time pin 4 of U3340 (digit four enable) goes HI. These two HI's reset the flip-flop through U3301A (the Q output goes LO). This LO is inverted by U3323C and allows Q3143 to conduct. This increases the gain of the integrator by a factor of ten (see Integrator Gain Switching in the Analog-to-Digital Converter discussion).

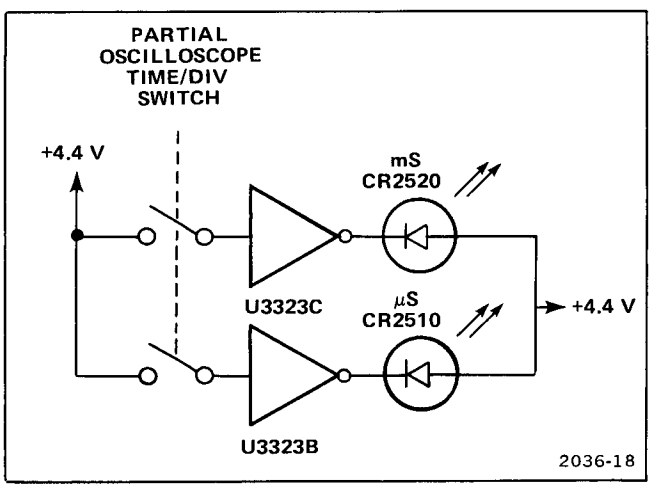


Fig. 4-20. Simplified diagram of ms and μs Logic when in the TIME function.

Overrange Condition

When an overrange condition does not exist, one of the digit enable outputs is always HI (pin 1, 2, 3, or 4 of U3340). The digit enable outputs are connected to two nor gates (U3383D and U3383C). Therefore, one of the nor gate outputs is always LO (see Figure 4-21). The nor gate outputs are connected to a nand gate (U3301B). With one input of U3301B always LO, its output is always HI.

When an overrange condition exists, circuitry within U3340 causes all four digit enable outputs to step LO at the same time, resetting the RS flip-flop through U3383D, U3383C, and U3301B. The Q output goes HI, is inverted through U3023C and turns off Q3143. This decreases the gain of the integrator by a factor of ten. (See Integrator Gain Switching in the Analog-to-Digital Converter discussion.)

POWER SUPPLY ◈8

The DM44 Power Supply is a floating supply that uses the accessory windings of the oscilloscope power transformer to provide the regulated voltages; +12 volts, +5 volts, and −12 volts.

The +12 Volt Supply is regulated by integrated circuit regulator U2614, which contains a reference voltage, output driver, buffers, etc.

The +5 Volt Supply is regulated by integrated circuit regulator U2624, which also contains a reference voltage, drivers, buffers, etc.

The −12 Volt Supply reference voltage is the +12 Volt Supply across R2635. Feedback from the junction of R2635 and R2634 is applied to the comparator composed of Q2638 and Q2634. Transistor Q2636 is the series regulator. Q2632 provides current limiting.

Ground 2 is the ground for the analog circuit and ground 1 is the digital ground return.

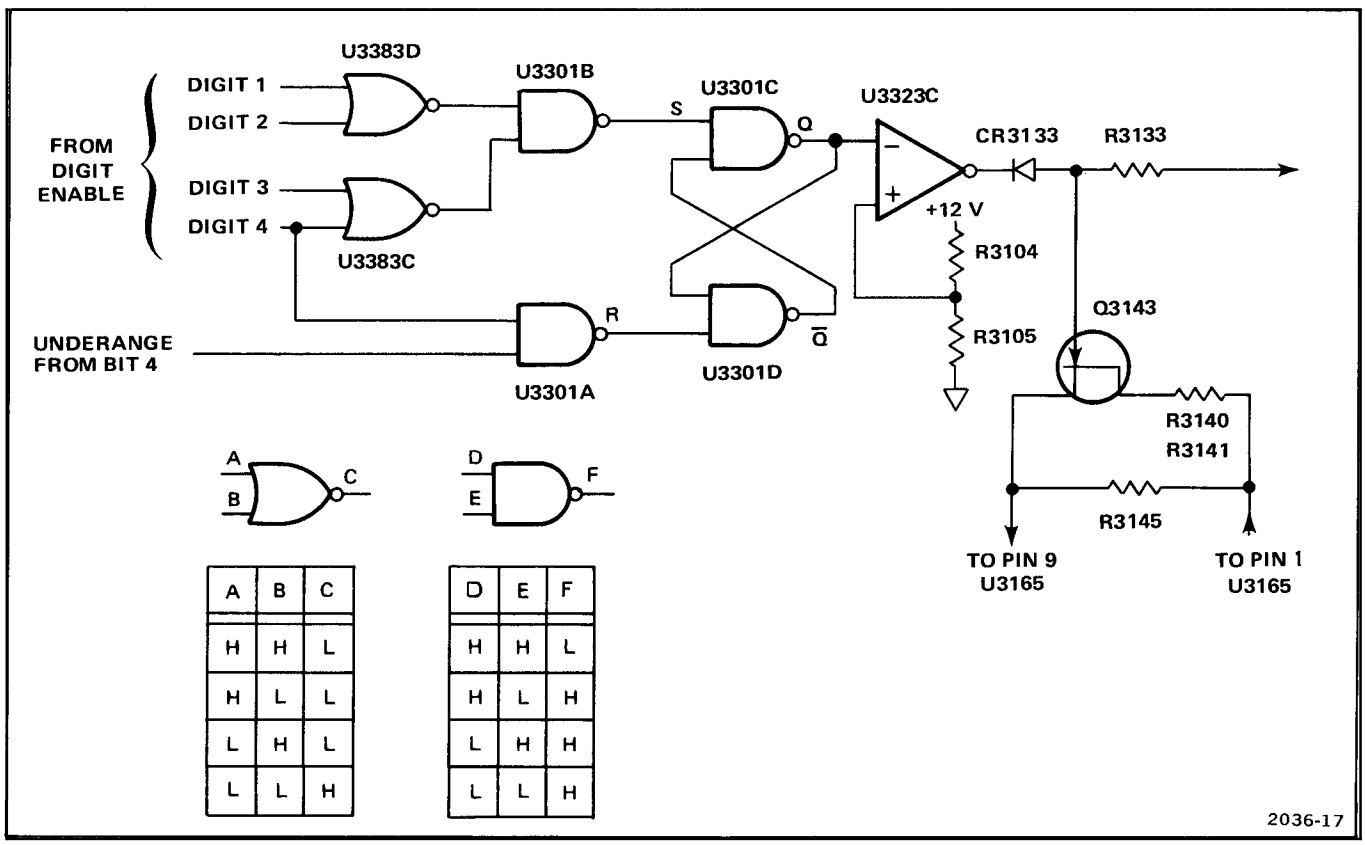


Fig. 4-21. Simplified diagram of TIME and 1/TIME Autorange Logic.

MAINTENANCE

This section contains information for use in corrective maintenance and instructions for user modifications. The preventive maintenance information found in the oscilloscope service manual also applies to the DM44 and will not be repeated here.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions.

1. Disconnect instrument from power source before removing or installing components.

2. Handle semiconductors with care. Many of the semiconductors used in this instrument, especially MOS types, can be damaged by static discharge. Static discharge damage may not be immediately apparent.

3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).

4. Do not use excessive heat when soldering. This can damage circuit boards and semiconductors.

CABINET REMOVAL

WARNING

To prevent electrical shock, disconnect power before removing the cabinet.

DM44 Cover

Use the following procedure to remove the DM44 cover.

1. Disconnect power cord.

2. Loosen screw at back of accessory pouch and slide pouch back off of the cabinet top. Remove two screws from the DM44 cover (see Figure 5-1).

3. Slide the DM44 cover toward the rear of the instrument to remove.

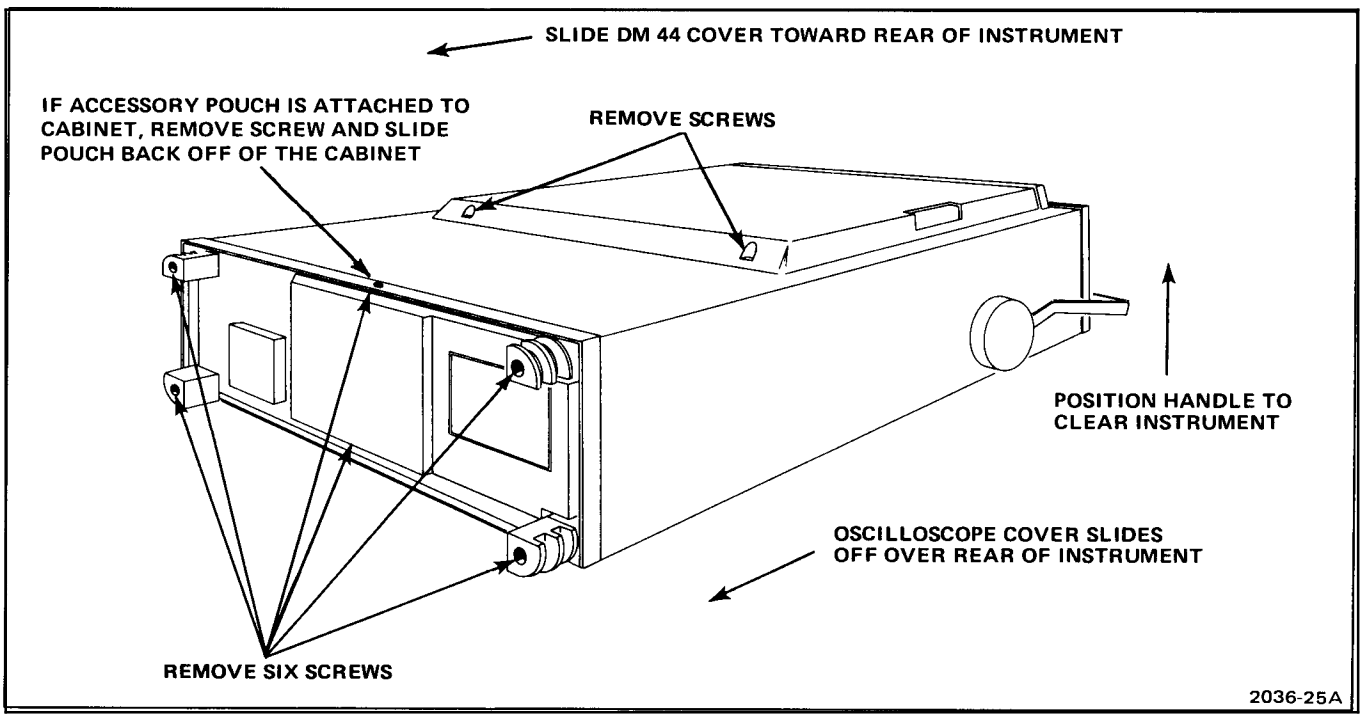


Fig. 5-1. Cover removal.

Oscilloscope Cabinet

Use the following procedure to remove the oscilloscope cabinet.

1. Disconnect the power cord.
2. Unwrap the power cord from the cord-wrap feet.
3. Remove the six screws as shown in Figure 5-1.
4. Remove the rear ring.
5. Install the oscilloscope front cover. Stand the instrument on its front cover on a flat surface.
6. Lift the cabinet to remove.

USER MODIFICATIONS

The following information gives instructions for making user modifications.

INPUT IMPEDANCE MODIFICATION

Use the following procedure to increase the input impedance to 1000 megohms in the 200-millivolt and 2-volt ranges of the VOLTS function.

1. Remove the DM44 cover (see Cabinet Removal).
2. Unsolder and remove the wire strap as shown in Figure 5-2.
3. Replace the DM44 cover.

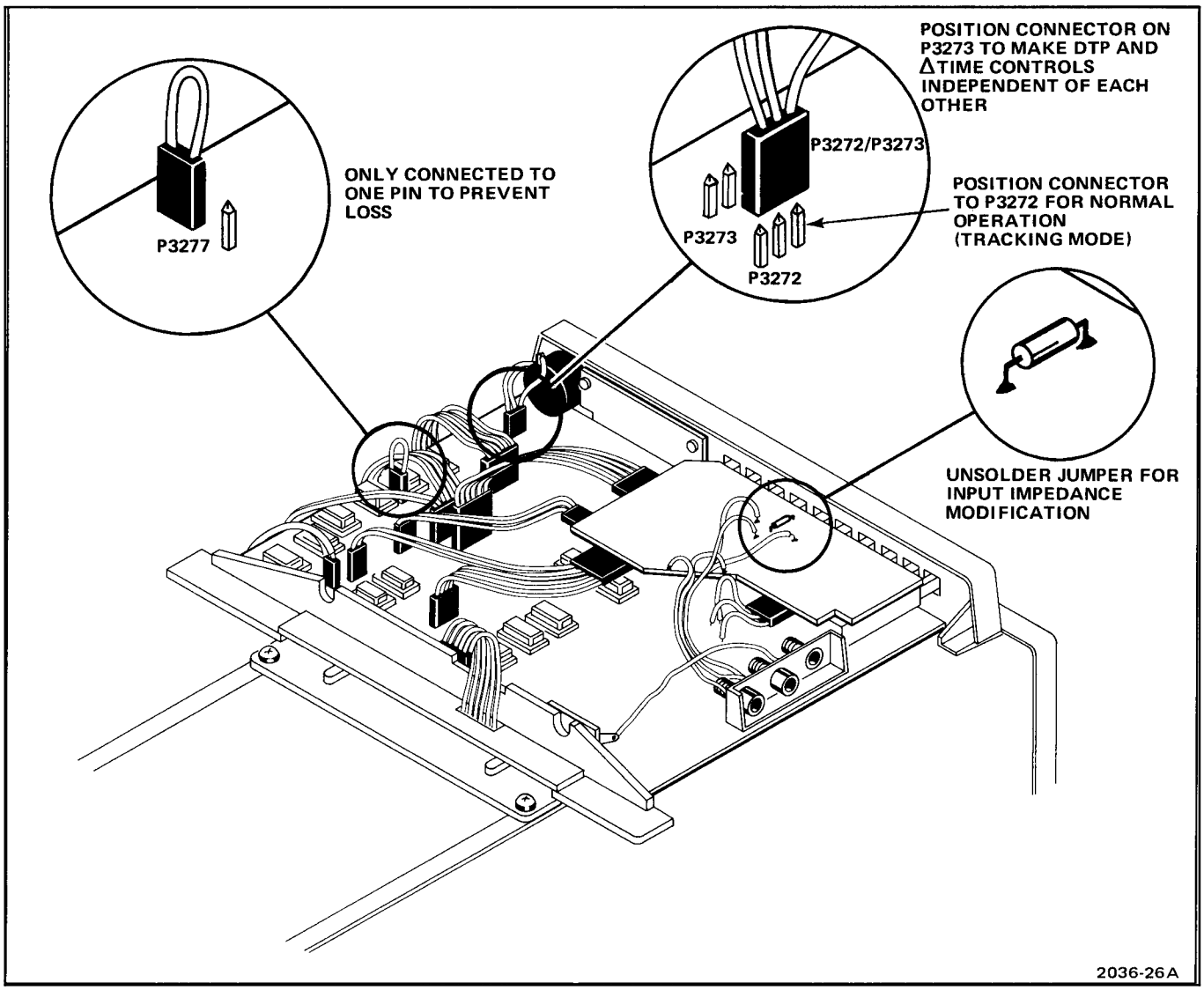
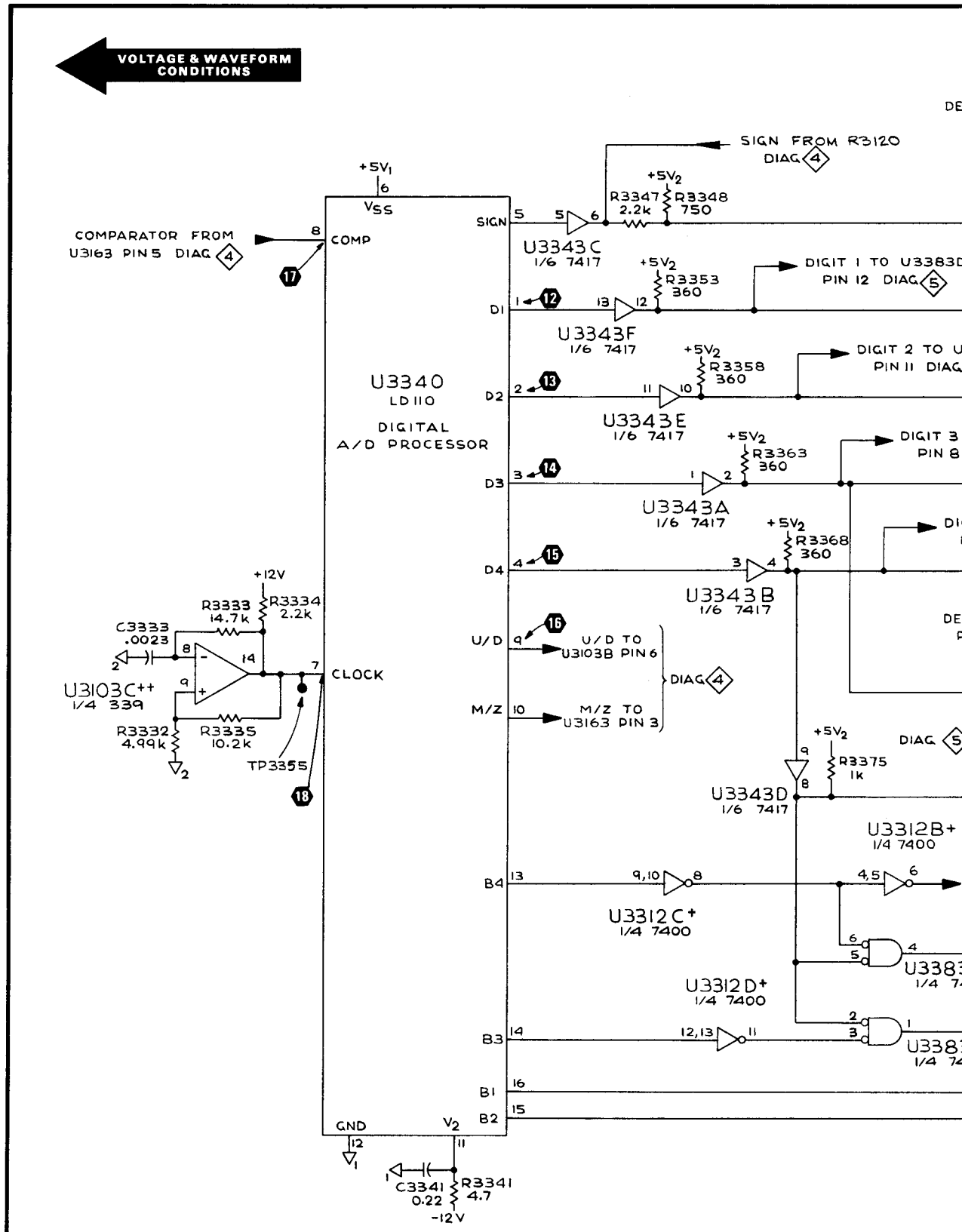
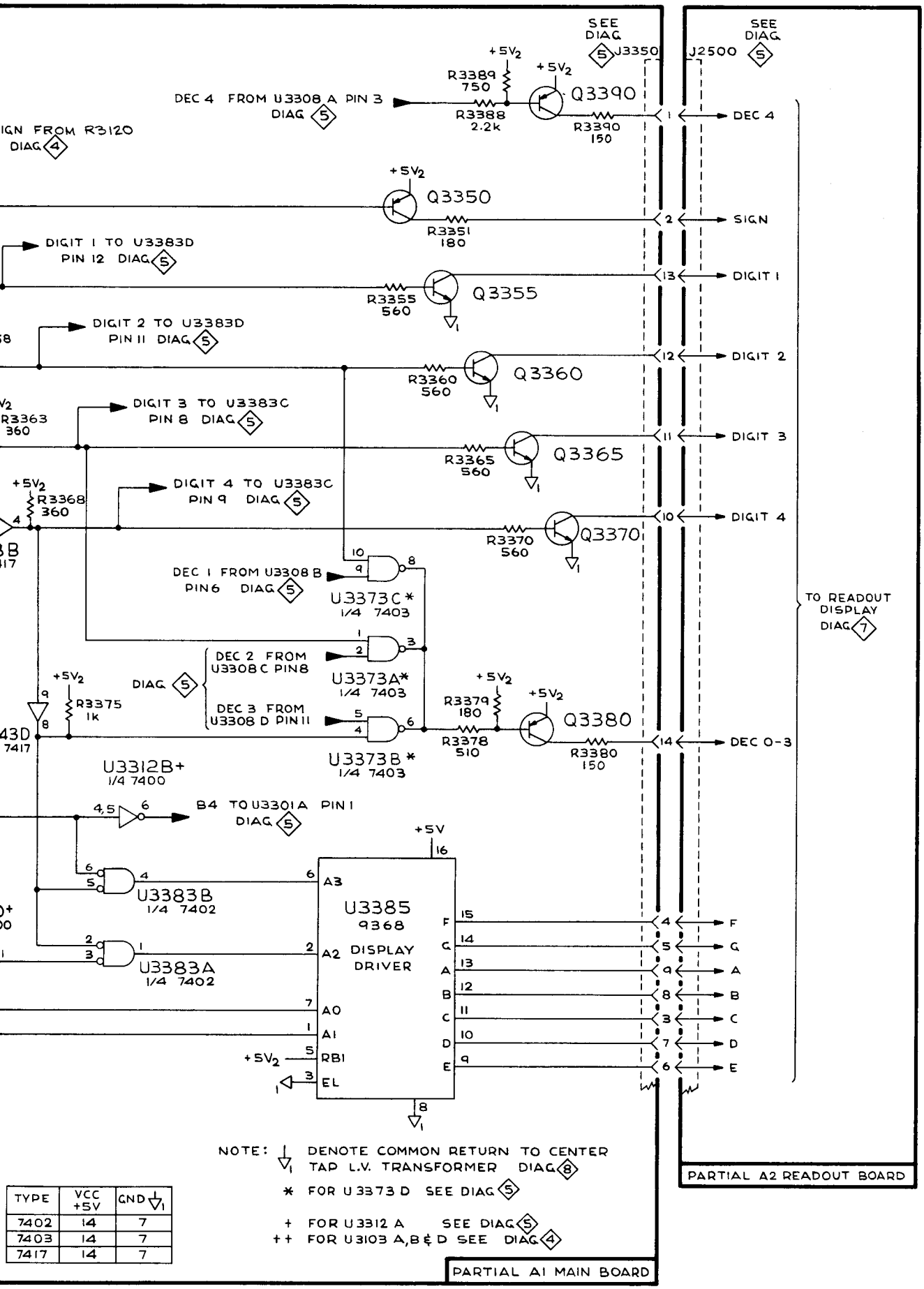


Fig. 5-2. User modification.



FOR COMPONENT LOCATION ILLUSTRATIONS:
A1 MAIN BOARD (LATE) . . . BACK OF DIAG. & ILLUS. PAGE
A1 MAIN BOARD (EARLY) . . BACK OF BLOCK DIAG.
A2 READOUT BOARD . . . . . BACK OF DIAG.1
A3 REGULATOR BOARD . . . BACK OF DIAG.1
A4 SWITCH BOARD . . . . . BACK OF DIAG.1

TYPE	VCC +5V	GND ⏚1
7402	14	7
7403	14	7
7417	14	7



TYPE	VCC +5V	GND
7402	14	7
7403	14	7
7417	14	7

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READOUT LOGIC 6

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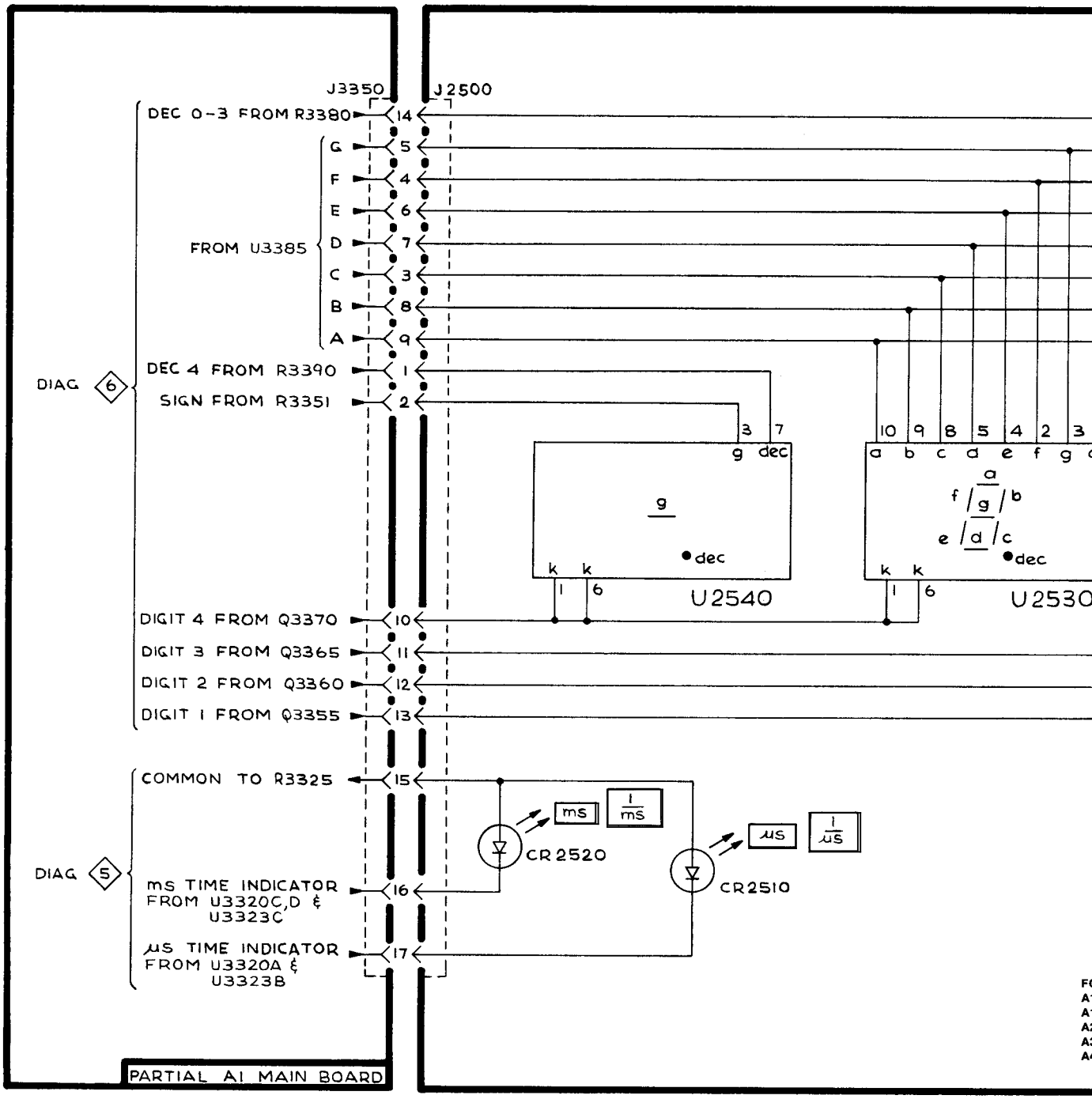

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REV. A

DM44

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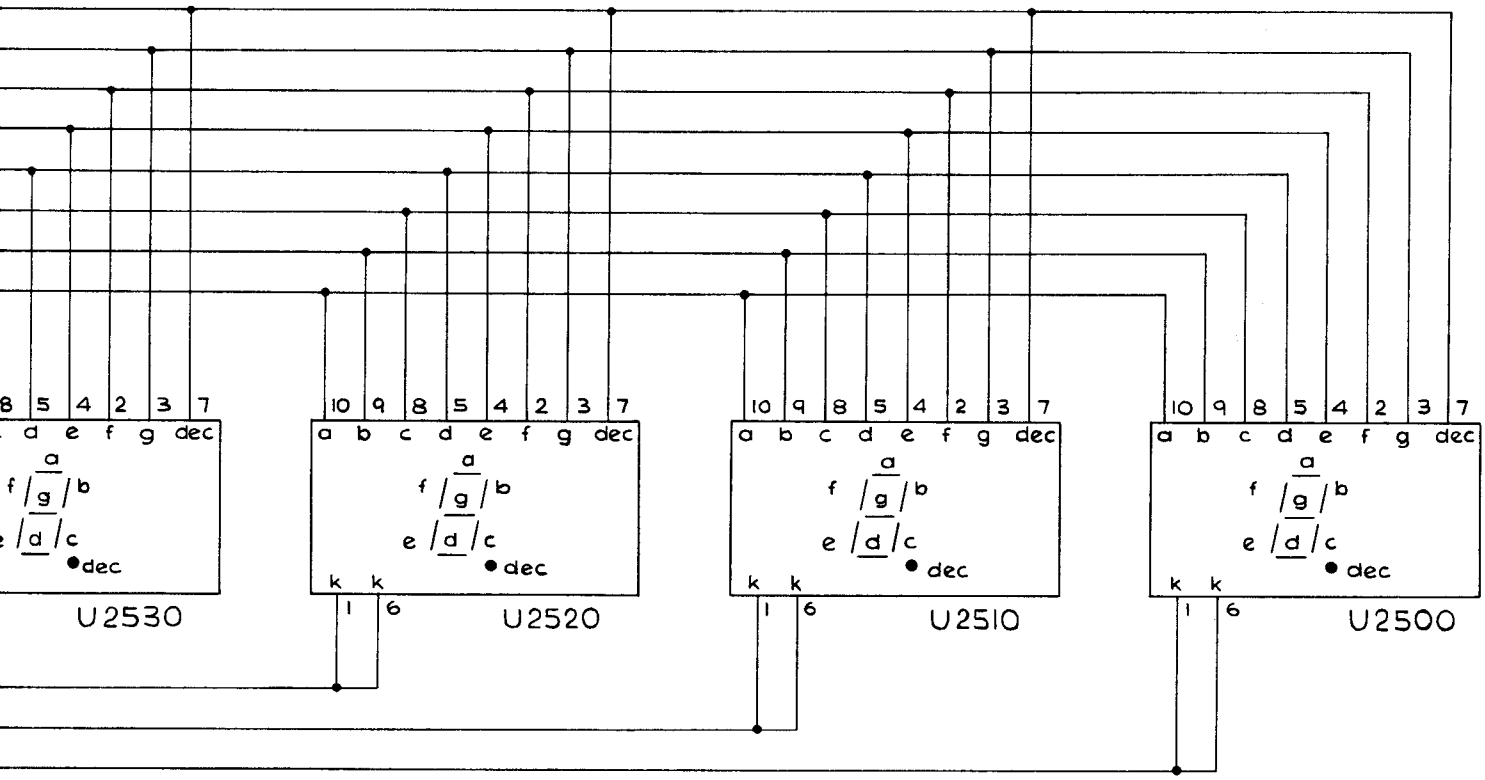

FOR COMPONENT LOCATION ILLUSTRATIONS:
A1 MAIN BOARD (LATE) . . . BACK OF DIAG. & ILLUS. PAGE
A1 MAIN BOARD (EARLY) . . BACK OF BLOCK DIAG.
A2 READOUT BOARD . . . . . BACK OF DIAG.1
A3 REGULATOR BOARD . . . BACK OF DIAG.1
A4 SWITCH BOARD . . . . . BACK OF DIAG.1

A2 READOUT BOARD

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REV. A, MARCH 1977

READOUT DISPLAY ◇7

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